

App. No. 10/608,295
Office Action Dated February 21, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Claims 1 and 13 are amended.

Claim 20 is new.

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a substrate;

a plurality of semiconductor chips mounted on the substrate by stacking one on top of another; and

an encapsulation resin layer,

wherein, among the plurality of semiconductor chips, a first semiconductor chip as an uppermost semiconductor chip is mounted with a surface thereof on which a circuit is formed facing the substrate, wherein the first semiconductor chip is directly and electrically connected to bumps and a second semiconductor chip provided immediately below the first semiconductor chip is directly and electrically connected to the bumps, and

wherein the encapsulation resin layer is formed so that at least a surface of the first semiconductor chip opposite to the surface on which the circuit is formed and a portion adjacent to said opposite surface in each of side surfaces of the first semiconductor chip are exposed to the outside of the encapsulation resin layer and the surface on which the circuit is formed and a remaining portion in each of the side surfaces are covered with the encapsulation resin layer.

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2. (Original) The semiconductor device according to claim 1, wherein, among the plurality of semiconductor chips, a lowermost semiconductor chip is bonded to the substrate with an adhesive.
3. (Previously Presented) The semiconductor device according to claim 1, wherein the bumps are formed from Ag, Au, Cu, or solder.
4. (Original) The semiconductor device according to claim 3, wherein a portion of the first semiconductor chip is bonded to a portion of the second semiconductor chip with an adhesive.
5. (Original) The semiconductor device according to claim 1, wherein, among the plurality of semiconductor chips, a lowermost semiconductor chip is electrically connected to the substrate via a wire.
6. (Original) The semiconductor device according to claim 3, wherein the bumps form a space between the first semiconductor chip and the second semiconductor chip, and the space is filled with the encapsulation resin of the encapsulation resin layer.
7. (Original) The semiconductor device according to claim 1, wherein the substrate is a lead frame.
8. (Original) The semiconductor device according to claim 7, wherein, among the plurality of semiconductor chips, a lowermost semiconductor chip is bonded to one surface of a die pad portion of the lead frame, and wherein the encapsulation resin layer is formed so the other surface of the die pad portion is exposed to the outside of the encapsulation resin layer.
9. (Original) The semiconductor device according to claim 1, wherein, on a second semiconductor chip provided immediately below the first semiconductor chip, a third semiconductor chip is mounted along with the first semiconductor chip.
10. (Original) The semiconductor device according to claim 9, wherein both the first semiconductor chip and the third semiconductor chip are electrically connected to the second semiconductor chip via bumps.

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11. (Original) The semiconductor device according to claim 1, wherein a heat dissipator is provided on the surface of the first semiconductor chip exposed to the outside of the encapsulation resin layer.
12. (Original) The semiconductor device according to claim 11, wherein the heat dissipator is a metal film or a metal heat sink.
13. (Withdrawn and Currently Amended) A method for manufacturing a semiconductor device comprising a substrate, a plurality of semiconductor chips mounted on the substrate by stacking one on top of another, and an encapsulation resin layer made of encapsulation resin, the method comprising the steps of:
- a. mounting a plurality of semiconductor chips on a substrate by stacking one on top of another so that a first semiconductor chip as an uppermost semiconductor chip is mounted with a surface thereof on which a circuit is formed facing the substrate; and
 - b. forming an encapsulation resin layer so that at least a surface of the first semiconductor chip opposite to the surface on which the circuit is formed and a portion adjacent to said opposite surface in each of side surfaces of the first semiconductor chip are exposed to the outside of the encapsulation resin layer and the surface on which the circuit is formed and a remaining portion in each of the side surfaces are covered with the encapsulation resin layer.
14. (Withdrawn) The method according to claim 13, wherein the step (b) is carried out by placing a stacked product obtained by mounting the plurality of semiconductor chips on the substrate in the step (a) in a mold having a space capable of accommodating the stacked product, and injecting or transferring the encapsulation resin into the space, the surface opposite to the surface on which the circuit is formed and the part of the side surfaces of the first semiconductor chip being allowed to be exposed to the outside of the encapsulation resin by:

attaching to a film member to a region opposing the first semiconductor chip in an inner wall of the mold that defines the space, and

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bringing the film member into intimate contact with the surface opposite to the surface on which the circuit is formed and the part of the side surfaces of the first semiconductor chip when injecting or transferring the encapsulation resin.

15. (Withdrawn) The method according to claim 14, wherein the mold comprises an upper half having a recess capable of accommodating at least the first semiconductor chip and the second semiconductor chip and a lower half having a recess that allows the substrate to fit therein, the film member is attached to an inner surface of the recess formed in the upper half so as to fit the shape of the inner surface, and the film member is brought into intimate contact with the surface opposite to the surface on which the circuit is formed and the part of the side surfaces of the first semiconductor chip by applying pressure between the upper half and the lower half.

16. (Withdrawn) The method according to claim 13, wherein, in the step (a) a second semiconductor chip provided immediately below the first semiconductor chip is mounted with a surface thereof on which a circuit is formed facing the first semiconductor chip, and the first semiconductor chip and the second semiconductor chip are electrically connected to each other via bumps.

17. (Withdrawn) The method according to claim 16, further comprising the step of filling an underfill material into a space formed between the first semiconductor chip and the second semiconductor chip by the bumps.

18. (Withdrawn) The method according to claim 16, wherein, in the step (a), an adhesive is applied to one portion of the surface of the second semiconductor chip on which the circuit is formed beforehand, and the first semiconductor chip is fixed to the second semiconductor chip with the adhesive.

19. (Withdrawn) The method according to claim 16, wherein the bumps form a space between the first semiconductor chip and the second semiconductor chip, and, in the step (b), the encapsulation resin layer is formed so that the space also is filled with the encapsulation resin for forming the encapsulation resin layer.

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20. (New) The semiconductor device according to claim 1, wherein each of the first semiconductor chip and the second semiconductor chip comprises a plurality of electrode pads, and

each of the electrode pads of the first semiconductor chip is connected to the corresponding electrode pad of the second semiconductor chip via a single bump.